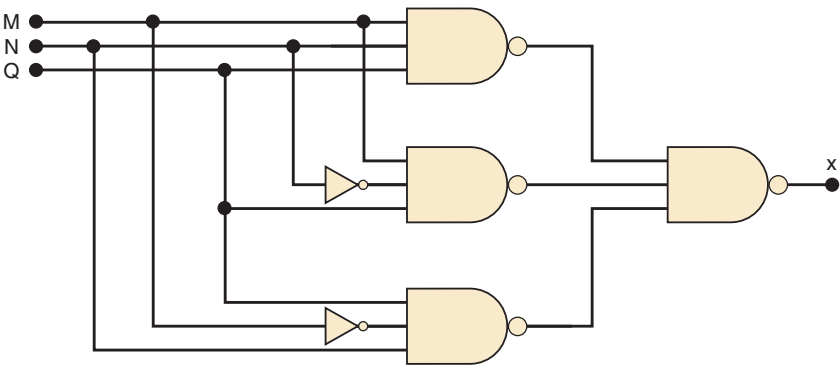


- (c) $w = ABC + A\overline{B}C + \overline{A}$
- (d) $q = \overline{RST}(\overline{R} + \overline{S} + \overline{T})$
- (e) $x = \overline{A}\overline{B}\overline{C} + \overline{A}BC + ABC + A\overline{B}\overline{C} + A\overline{B}C$
- (f) $z = (B + \overline{C})(\overline{B} + C) + \overline{A} + B + \overline{C}$
- (g) $y = (\overline{C} + \overline{D}) + \overline{A}CD + A\overline{B}\overline{C} + \overline{A}\overline{B}CD + ACD$
- (h) $x = AB(\overline{C}D) + \overline{A}BD + \overline{B}\overline{C}D$

B 4-2. Simplify the circuit of Figure 4-68 using Boolean algebra.

FIGURE 4-68 Problems 4-2 and 4-3.



B 4-3* Change each gate in Problem 4-2 to a NOR gate, and simplify the circuit using Boolean algebra.

SECTION 4-4

B, D 4-4* Design the logic circuit corresponding to the truth table shown in Table 4-11.

TABLE 4-11

A	B	C	x
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

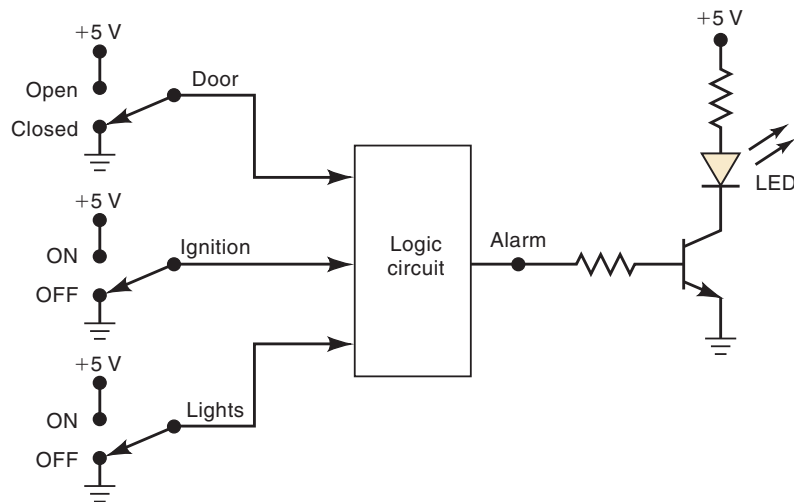
- B, D** 4-5. Design a logic circuit whose output is HIGH *only* when a majority of inputs A, B, and C are LOW.
- D** 4-6. A manufacturing plant needs to have a horn sound to signal quitting time. The horn should be activated when either of the following conditions is met:
1. It's after 5 o'clock and all machines are shut down.
 2. It's Friday, the production run for the day is complete, and all machines are shut down.

Design a logic circuit that will control the horn. (*Hint:* Use four logic input variables to represent the various conditions; for example,

input A will be HIGH only when the time of day is 5 o'clock or later.)

- D** 4-7* A four-bit binary number is represented as $A_3A_2A_1A_0$, where A_3 , A_2 , A_1 , and A_0 represent the individual bits and A_0 is equal to the LSB. Design a logic circuit that will produce a HIGH output whenever the binary number is greater than 0010 and less than 1000.
- D** 4-8. Figure 4-69 shows a diagram for an automobile alarm circuit used to detect certain undesirable conditions. The three switches are used

FIGURE 4-69 Problem 4-8.



to indicate the status of the door by the driver's seat, the ignition, and the headlights, respectively. Design the logic circuit with these three switches as inputs so that the alarm will be activated whenever either of the following conditions exists:

- The headlights are on while the ignition is off.
- The door is open while the ignition is on.

4-9* Implement the circuit of Problem 4-4 using all NAND gates.

4-10. Implement the circuit of Problem 4-5 using all NAND gates.

SECTION 4-5

- B** 4-11. Determine the minimum expression for each K map in Figure 4-70. Pay particular attention to step 5 for the map in (a).

FIGURE 4-70 Problem 4-11.

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1	1	1	1
$\bar{A}B$	1	1	0	0
AB	0	0	0	1
$A\bar{B}$	0	0	1	1

(a)*

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1	0	1	1
$\bar{A}B$	1	0	0	1
AB	0	0	0	0
$A\bar{B}$	1	0	1	1

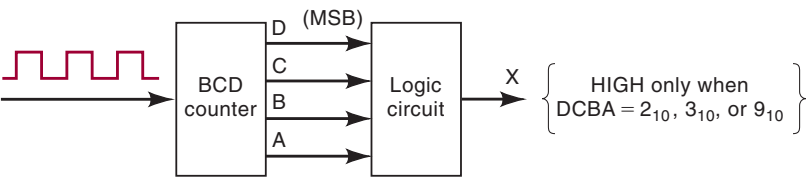
(b)

	$\bar{C}$	C
$\bar{A}\bar{B}$	1	1
$\bar{A}B$	0	0
AB	1	0
$A\bar{B}$	1	X

(c)

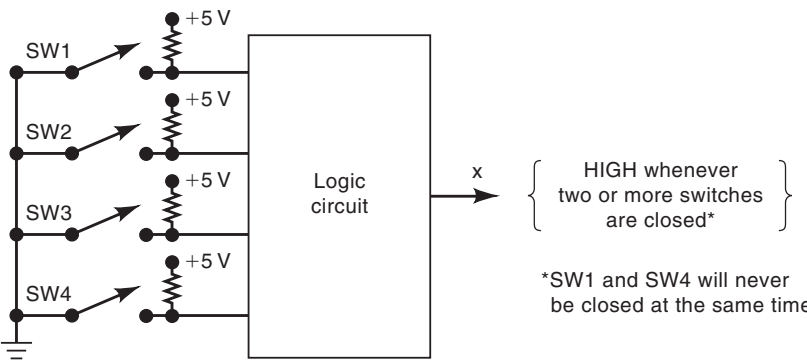
- B** 4-12. For the truth table below, create a 2×2 K map, group terms, and simplify. Then look at the truth table again to see if the expression is true for every entry in the table.
- | A | B | y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |
- B** 4-13. Starting with the truth table in Table 4-11, use a K map to find the simplest SOP equation.
- B** 4-14. Simplify the expression in (a)* Problem 4-1(e) using a K map. (b) Problem 4-1(g) using a K map. (c)* Problem 4-1(h) using a K map.
- B** 4-15* Obtain the output expression for Problem 4-7 using a K map.
- C, D** 4-16. Figure 4-71 shows a *BCD counter* that produces a four-bit output representing the BCD code for the number of pulses that have been applied to the counter input. For example, after four pulses have occurred, the counter outputs are $DCBA = 0100_2 = 4_{10}$. The counter resets to 0000 on the tenth pulse and starts counting over again. In other words, the $DCBA$ outputs will never represent a number greater than $1001_2 = 9_{10}$.
- (a)* Design the logic circuit that produces a HIGH output whenever the count is 2, 3, or 9. Use K mapping and take advantage of the don't-care conditions.
- (b) Repeat for $x = 1$ when $DCBA = 3, 4, 5, 8$.

FIGURE 4-71 Problem 4-16.



- D** 4-17* Figure 4-72 shows four switches that are part of the control circuitry in a copy machine. The switches are at various points along the path of the copy paper as the paper passes through the machine. Each switch is normally open, and as the paper passes over a switch, the switch closes. It is impossible for switches SW1 and SW4 to be closed at the same time. Design the logic circuit to produce a HIGH output whenever *two or more* switches are closed at the same time. Use K mapping and take advantage of the don't-care conditions.

FIGURE 4-72 Problem 4-17.

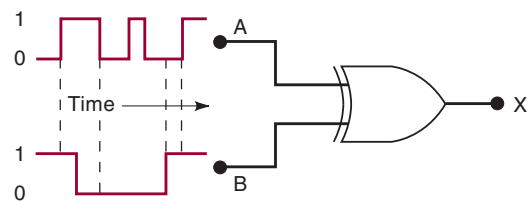


- D** 4-18* Example 4-3 demonstrated algebraic simplification. Step 3 resulted in the SOP equation $z = \overline{A}BC + \overline{A}CD + \overline{A}BCD + ABC$. Use a K map to prove that this equation can be simplified further than the answer shown in the example.
- C** 4-19. Use Boolean algebra to arrive at the same result obtained by the K map method of Problem 4-18.

SECTION 4-6

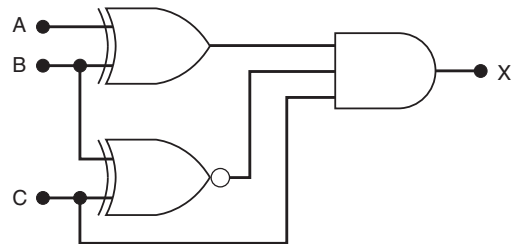
- B** 4-20. (a) Determine the output waveform for the circuit of Figure 4-73.
(b) Repeat with the B input held LOW.
(c) Repeat with B held HIGH.

FIGURE 4-73 Problem 4-20.



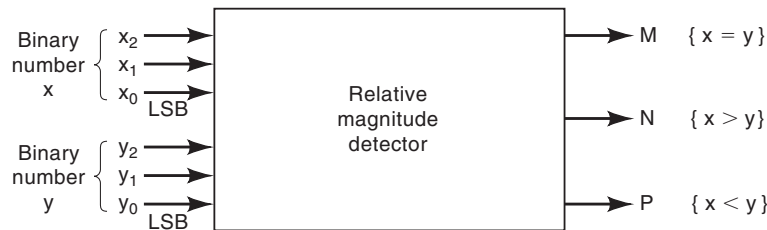
- B** 4-21* Determine the input conditions needed to produce $x = 1$ in Figure 4-74.

FIGURE 4-74 Problem 4-21.

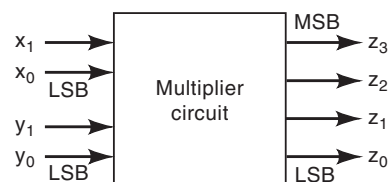


- B** 4-22. Design a circuit that produces a HIGH output only when all three inputs are the same level.
(a) Use a truth table and K map to produce the SOP solution.
(b) Use two-input XOR and other gates to find a solution. (*Hint:* Recall the transitive property from algebra... if $a = b$ and $b = c$ then $a = c$.)
- B** 4-23* A 7486 chip contains four XOR gates. Show how to make an XNOR gate using only a 7486 chip. *Hint:* See Example 4-16.
- B** 4-24* Modify the circuit of Figure 4-23 to compare two four-bit numbers and produce a HIGH output when the two numbers match exactly.
- B** 4-25. Figure 4-75 represents a *relative-magnitude detector* that takes two three-bit binary numbers, $x_2x_1x_0$ and $y_2y_1y_0$, and determines whether they are equal and, if not, which one is larger. There are three outputs, defined as follows:
1. $M = 1$ only if the two input numbers are equal.
 2. $N = 1$ only if $x_2x_1x_0$ is greater than $y_2y_1y_0$.
 3. $P = 1$ only if $y_2y_1y_0$ is greater than $x_2x_1x_0$.

Design the logic circuitry for this detector. The circuit has *six* inputs and *three* outputs and is therefore much too complex to handle using the truth table approach. Refer to Example 4-17 as a hint about how you might start to solve this problem.

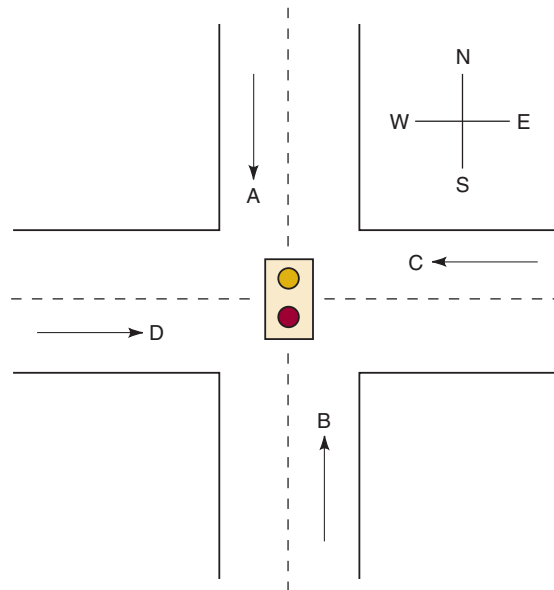
FIGURE 4-75 Problem 4-25.**MORE DESIGN PROBLEMS**

- C, D** 4-26* Figure 4-76 represents a multiplier circuit that takes two-bit binary numbers, x_1x_0 and y_1y_0 , and produces an output binary number $z_3z_2z_1z_0$ that is equal to the arithmetic product of the two input numbers. Design the logic circuit for the multiplier. (*Hint:* The logic circuit will have four inputs and four outputs.)

FIGURE 4-76 Problem 4-26.

- D** 4-27. A BCD code is being transmitted to a remote receiver. The bits are A_3, A_2, A_1 , and A_0 , with A_3 as the MSB. The receiver circuitry includes a *BCD error detector* circuit that examines the received code to see if it is a legal BCD code (i.e., ≤ 1001). Design this circuit to produce a HIGH for any error condition.
- D** 4-28* Design a logic circuit whose output is HIGH whenever A and B are both HIGH as long as C and D are either both LOW or both HIGH. Try to do this without using a truth table. Then check your result by constructing a truth table from your circuit to see if it agrees with the problem statement.
- D** 4-29. Four large tanks at a chemical plant contain different liquids being heated. Liquid-level sensors are being used to detect whenever the level in tank A or tank B rises above a predetermined level. Temperature sensors in tanks C and D detect when the temperature in either of these tanks drops below a prescribed temperature limit. Assume that the liquid-level sensor outputs A and B are LOW when the level is satisfactory and HIGH when the level is too high. Also, the temperature-sensor outputs C and D are LOW when the temperature is satisfactory and HIGH when the temperature is too low. Design a logic circuit that will detect whenever the level in tank A or tank B is too high at the same time that the temperature in either tank C or tank D is too low.
- C, D** 4-30* Figure 4-77 shows the intersection of a main highway with a secondary access road. Vehicle-detection sensors are placed along lanes C and D (main road) and lanes A and B (access road). These sensor

FIGURE 4-77 Problem 4-30.



outputs are LOW (0) when no vehicle is present and HIGH (1) when a vehicle is present. The intersection traffic light is to be controlled according to the following logic:

1. The east-west (E-W) traffic light will be green whenever *both* lanes *C* and *D* are occupied.
2. The E-W light will be green whenever *either* *C* or *D* is occupied but lanes *A* and *B* are not *both* occupied.
3. The north-south (N-S) light will be green whenever *both* lanes *A* and *B* are occupied but *C* and *D* are not *both* occupied.
4. The N-S light will also be green when *either* *A* or *B* is occupied while *C* and *D* are *both* vacant.
5. The E-W light will be green when *no* vehicles are present.

Using the sensor outputs *A*, *B*, *C*, and *D* as inputs, design a logic circuit to control the traffic light. There should be two outputs, N-S and E-W, that go HIGH when the corresponding light is to be *green*. Simplify the circuit as much as possible and show *all* steps.

SECTION 4-7

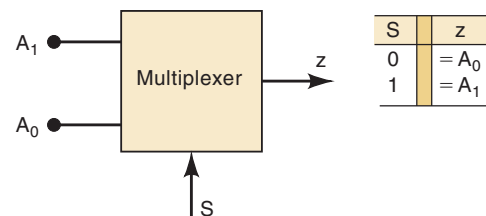
- D** 4-31. Redesign the parity generator and checker of Figure 4-25 to (a) operate using odd parity. (*Hint*: What is the relationship between an odd-parity bit and an even-parity bit for the same set of data bits?) (b) Operate on eight data bits.

SECTION 4-8

- B** 4-32. (a) Under what conditions will an OR gate allow a logic signal to pass through to its output unchanged?
 (b) Repeat (a) for an AND gate.
 (c) Repeat for a NAND gate.
 (d) Repeat for a NOR gate.
- B** 4-33* (a) Can an INVERTER be used as an enable/disable circuit? Explain.
 (b) Can an XOR gate be used as an enable/disable circuit? Explain.

- D** 4-34. Design a logic circuit that will allow input signal A to pass through to the output only when control input B is LOW while control input C is HIGH; otherwise, the output is LOW.
- D** 4-35* Design a circuit that will *disable* the passage of an input signal only when control inputs B , C , and D are all HIGH; the output is to be HIGH in the disabled condition.
- D** 4-36. Design a logic circuit that controls the passage of signal A according to the following requirements:
1. Output X will equal A when control inputs B and C are the same.
 2. X will remain HIGH when B and C are different.
- D** 4-37. Design a logic circuit that has two signal inputs, A_1 and A_0 , and a control input S so that it functions according to the requirements given in Figure 4-78. (This type of circuit is called a *multiplexer* and will be covered in Chapter 9.)

FIGURE 4-78 Problem 4-37.

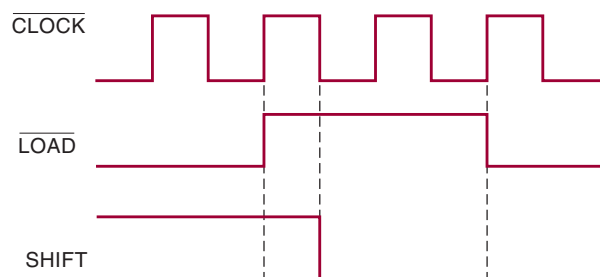


- D** 4-38* Use K mapping to design a circuit to meet the requirements of Example 4-17. Compare this circuit with the solution in Figure 4-23. This points out that the K-map method cannot take advantage of the XOR and XNOR gate logic. The designer must be able to determine when these gates are applicable.

SECTIONS 4-9 TO 4-13

- T*** 4-39. (a) A technician testing a logic circuit sees that the output of a particular INVERTER is stuck LOW while its input is pulsing. List as many possible reasons as you can for this faulty operation.
- (b) Repeat part (a) for the case where the INVERTER output is stuck at an indeterminate logic level.
- T** 4-40* The signals shown in Figure 4-79 are applied to the inputs of the circuit of Figure 4-32. Suppose that there is an internal open circuit at Z1-4.
- (a) What will a logic probe indicate at Z1-4?
 - (b) What dc voltage reading would you expect at Z1-4? (Remember that the ICs are TTL.)

FIGURE 4-79 Problem 4-40.



*Recall that T indicates a troubleshooting exercise.